Paper No. 25

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte SUNIL MEHTA

Appeal No. 2000-0160
Application 08/595,150[1]

ON BRIEF

Before BARRETT, GROSS, and BLANKENSHIP, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the

BACKGROUND

The invention relates to an integrated circuit and a method of fabricating an integrated circuit. The disclosed invention is described in Appellant's brief, pages 3-4.

Claim 19 is reproduced below.

> 19. An integrated circuit having a plurality of semiconductor devices therein and a multilevel metallization structure for interconnection of said semiconductor devices thereon, said multilevel metallization structure comprising,
>
> a plurality of substantially parallel, separated, patterned metal layers, each said metal layer being separated by an interlevel dielectric (ILD) layer of silicon dioxide therebetween, said patterned metal layers being comprised of electrically conducting lines, said electrically conducting lines having top surfaces and edge surfaces;
>
> said interlevel dielectric layers between said metal layers having vias therethrough, each said via having via sidewalls 55 and a via bottom end surface 57, wherein at least one of said vias has a first portion of said via bottom end surface 57 being contiguous with a portion of said top surface of one of said electrically conducting lines and a second portion of said via bottom end surface 57 being above a portion of said edge surface of said one of said electrically conducting lines, said one via thereby being misaligned with respect to said one of said electrically conducting lines, said vias having conducting via plugs therein, said via plugs providing electrical connectivity between said metal layers;
>
> one or more of said metal layers having an insulating ILD via etch stop cap layer contiguously thereon, said etch

The Examiner relies on the following references:

Barber et al. (Barber)	4,966,870	October 30, 1990
Woo et al. (Woo)	5,451,543	September 19, 1995
Aoyama et al. (Aoyama)	5,592,024	January 7, 1997 (filed October 28, 1994)
Kalnitsky (European Patent Application)	EP 0 523 856	January 20, 1993

Claims 19-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Woo and Kalnitsky.

Claims 26, 28, 30, 32, and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Woo and Kalnitsky, further in view of Aoyama or Barber.

We refer to the Office action (Paper No. 16), the final rejection (Paper No. 18), and the examiner's answer (Paper No. 24) for a statement of the Examiner's rejection, and to the brief (Paper No. 23) for a statement of Appellant's arguments thereagainst.

OPINION

New grounds of rejection pursuant to 37 CFR § 1.196(b)

A claim which omits matter disclosed to be essential to the invention as described in the specification or in other statements of record is subject to rejection under 35 U.S.C.

356, 358 (CCPA 1976) (claims which failed to recite the use of a cooling zone, specially located, which the specification taught as essential, was not supported by enabling disclosure); In re Venezia, 530 F.2d 956, 959, 189 USPQ 149, 152 (CCPA 1976) (since all of the essential parts of the "kit" are recited in the claims, there is no basis for holding the claims incomplete); and In re Collier, 397 F.2d 1003, 1005, 158 USPQ 266, 268 (CCPA 1968) (claim failed to interrelate essential elements and failed to distinctly claim what appellant in his brief insisted was his invention). See also Reiffin v. Microsoft Corp., 48 USPQ2d 1274, 1277 (N.D. Cal. 1998) (omitted elements test), rev'd, remanded on other grounds 214 F.3d 1342, 54 USPQ2d 1915 (Fed. Cir. 2000); and Manual of Patent Examining Procedure §§ 2172, 2172.01.

Claims 19-21, 24, 26, 28, 30, and 34 are rejected under 35 U.S.C. § 112, first paragraph, as failing to recite an essential element and, therefore, as based on a lack of enabling disclosure. Claims 19 and 24 do not recite the electrically conducting coating 34 which is chemically inert with respect to reactants and reaction products of the Blanket Tungsten CVD via fill process. This layer is essential because otherwise the top

enabling disclosure under § 112, first paragraph. See Mayhew, 527 F.2d at 1233, 188 USPQ at 358. Claim 22 recites the inert coating; therefore, claims 22, 23, and 32 are not rejected.

Claims 19-24, 26, 28, 30, 32, and 34 are rejected under § 112, second paragraph, as failing to particularly point out and distinctly claim the subject matter which Appellant regards as his invention. First, it is clear from Appellant's brief that Appellant regards his invention as including the inert coating. Absent an inert electrically conducting coating, there is nothing to protect the exposed metal surfaces from damaging interactions with chemicals that lead to the problem of exploding vias as argued by Appellant (Br5-8). The claims are properly rejected under § 112, second paragraph, as failing to distinctly claim what Appellant in his brief insists is his invention.

Second, the absence of the inert coating in the claims causes a potential indefiniteness problem. Since there is no chemically inert electrically conducting coating 34 claimed as part of the patterned metal layers, the coating 34 and metal interconnect line 6 together are a "patterned metal layer" which has a top surface and edge surfaces and the via bottom end

indefiniteness.) The etch stop cap layer 54 does not completely cover the edge of this composite patterned metal layer because of overetching, as shown in Appellant's figures 8 and 9 and described in the specification, page 10, lines 10-13. Thus, to the extent Appellant asserts that the limitation of "said contiguous etch stop cap layer covering said electrically conducting edge surfaces" in claim 19 means "completely covering the edge surfaces," the limitation is misdescriptive of the disclosed invention under § 112, second paragraph. In the obviousness rejection, we have interpreted the limitation to require only covering part of the edge to avoid an indefiniteness problem and to be consistent with the disclosure. Claim 22, which specifies the electrically conducting coating on metal lines, does not clarify what part of the edge surface is covered by the etch stop cap layer. Claim 24 recites "not entirely removing said insulating ILD via etch stop cap layer covering said edge surfaces of said electrically conducting lines," which indicates that part of the edge surface may be exposed. Thus, claims 24 and 34 are not rejected under this second ground.

Third, the limitation of "a second portion of said via

It is not clear what is intended by "above a portion of said edge surface" or how this supports the "whereby" limitation. The edge surface is a vertical surface, so a "portion of said edge surface" must be on the vertical surface, and a surface "above" this is apparently vertically "above" the vertical edge surface. It is not clear how this defines the invention. We cannot tell whether Appellant intends to claim that the second portion of the via bottom end surface is below the level of the top surface.

Obviousness

Claims 19-23, 26, 28, 30, and 32

Claims 19-23, 26, 28, 30, and 32 are argued to stand or fall together as a group (Br4). Claim 19 is the independent claim.

The Examiner does not particularly identify the difference(s) between Woo and the subject matter of claim 19. The Examiner concludes that "one of ordinary skill in the art would have been motivated to select silicon nitride as a material for an etch stop cap layer 29 of Woo et al, and silicon oxide as a material for an interlevel dielectric layer 16 of Woo et al for the purpose of protecting the metal layers from damaging

to be a silicon nitride etch stop layer and a silicon oxide interlevel dielectric (ILD) layer. However, Woo discloses silicon nitride as an etch stop layer (e.g. col. 4, line 13) and discloses silicon-oxide based materials for the ILD layer (col. 4, lines 36-41). Woo does not mention silicon dioxide as a silicon-oxide based ILD material. Presumably, the Examiner was just careless in stating "silicon oxide" in the rejection instead of "silicon dioxide." Therefore, we assume that Kalnitsky is applied mainly to show silicon dioxide as an ILD material.

Appellant does not challenge the obviousness of using silicon dioxide as an ILD material in Woo.

Appellant argues (Br6) that neither Woo nor Kalnitsky teaches or suggests "said contiguous etch stop cap layer covering said electrically conducting edge surfaces" (claim 19).

We interpret "covering said electrically conducting edge surfaces" to require only partly covering the conducting edge. This interpretation is consistent with Appellant's figures 8 and 9, which show the etch stop cap layer 54 partially exposing the electrically conducting coating 34 which forms part of the electrically conducting edge surface. Because claim 19 does not

composite of metal interconnects 6 and metal coating 34. Woo teaches the etch stop layer 29 covering part of the edge of the conductor 10 (col. 7, lines 40-46) and so teaches "covering said electrically conducting edge surfaces."

Appellant argues that Woo's structure, because of the exposed metal edge, will result in damaging interactions with the chemicals used in via fill (Br5). It is argued that neither Woo nor Kalnitsky recognize or address the problem of exploding vias due to misalignment solved by Appellant, and neither of their structures would solve the problem (Br7-8).

These arguments are not commensurate in scope with claim 19. Claim 19 does not recite the specific metal for the metal layers or recite any properties thereof, such as being chemically inert, except that they form electrically conducting lines. Thus, the claim does not recite a structure that will have an exploding via problem. Moreover, claim 19 is to a structure and does not recite how the via plug is formed and does not recite that the via plug is formed by a Blanket Tungsten CVD process where tungsten hexafluoride or hydrogen fluoride will react with the exposed interconnect metal to have an exploding via problem.

Claims 24 and 34

Claims 24 and 34 stand or fall together.

The Examiner relies on the same reasoning for claim 24 as for claim 19. However, there are several differences between claim 19 and the product manufactured by the method of claim 24.

Claim 24 recites "depositing an ILD dielectric [sic, the term "dielectric" is redundant] layer over said insulating ILD via etch stop cap layer," but does not recite that the ILD layer is silicon dioxide as in claim 19. The fact that claim 24 recites an ILD via etch stop cap layer "made from a material which is substantially non-volatilized by silicon dioxide etchants" does not require a silicon dioxide ILD layer. Claim 24 recites "not entirely removing said insulating ILD via etch stop cap layer covering said edge surfaces of said electrically conducting lines," which expressly indicates that a part of the edge surface may be exposed, whereas we interpreted "covering" in claim 19 to only require "partially covering." Thus, the product produced by claim 24 is broader in these two respects than claim 19. Claim 24 recites the function "for protecting said

inherent result of the process specified in claim 24 (Br8) is not persuasive because of these differences.

Because claim 24 does not expressly require a silicon dioxide ILD layer, Kalnitsky is not needed. Woo teaches a silicon nitride etch stop layer which satisfies the limitation of an ILD via etch stop cap layer "made from a material which is substantially non-volatilized by silicon dioxide etchants."

Woo discloses that only a portion of the vertical sidewall needs to be exposed, which meets the limitation of "not entirely removing said insulating ILD via etch stop cap layer covering said edge surfaces of said electrically conducting lines." The unexposed edge surfaces in Woo perform the function "for protecting said edge surfaces from damaging interaction with chemicals associated with subsequent process steps" just as the unexposed edge surfaces are protected in the disclosed invention.

For these reasons, we conclude that claim 24 would have been obvious over Woo alone and that Appellant has failed to show error in the Examiner's rejection. The reliance on Woo alone does not create a new ground of rejection. See In re Bush, 296 F.2d 491, 496, 131 USPQ 263, 266-67 (CCPA 1961) ("the answer

rejection on a new ground"). The rejections of claims 24 and 34 are sustained.

CONCLUSION

The rejections of claims 19-24, 26, 28, 30, 32, and 34 are sustained.

New grounds of rejection have been entered as to claims 19-24, 26, 28, 30, 32, and 34 pursuant to 37 CFR § 1.196(b).

In addition to affirming the Examiner's rejection of one or more claims, this decision contains a new ground of rejection pursuant to 37 CFR § 1.196(b)(amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53,131, 53,197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)). 37 CFR § 1.196(b) provides, "A new ground of rejection shall not be considered final for purposes of judicial review."

Regarding any affirmed rejection, 37 CFR § 1.197(b) provides:

> (b) Appellant may file a single request for rehearing within two months from the date of the original decision . . . .

rejection to avoid termination of proceedings (37 CFR § 1.197(c)) as to the rejected claims:

> (1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner. . . .
>
> (2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record. . . .

Should Appellant elect to prosecute further before the Primary Examiner pursuant to 37 CFR § 1.196(b)(1), in order to preserve the right to seek review under 35 U.S.C. §§ 141 or 145 with respect to the affirmed rejection, the effective date of the affirmance is deferred until conclusion of the prosecution before the Examiner unless, as a mere incident to the limited prosecution, the affirmed rejection is overcome.

If Appellant elects prosecution before the Examiner and this does not result in allowance of the application, abandonment or a second appeal, this case should be returned to the Board of Patent Appeals and Interferences for final action on the affirmed rejection, including any timely request for rehearing thereof.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED - 37 CFR § 1.196(b)

LEE E. BARRETT Administrative Patent Judge	)
ANITA PELLMAN GROSS Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
HOWARD B. BLANKENSHIP Administrative Patent Judge	)

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